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Electrical property of pentacene organic thin-film transistors with a complementary-gated structure

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Abstract Organic thin-film transistors (OTFTs) are being extensively studied for the next generation electronic devices, which will require cost reduction and flexibility. In this study, OTFTs with a double-gated structure were fabricated and their electric properties depending on main and complementary gate voltages were presented. Not only the drain currents, but also the surface potentials of pentacene films were remarkably modulated in accordance with the complementary gate field. A pMOS d-inverter circuit constructed with conventional and double-gated OTFTs was designed and fabricated, and the gain of the d-inverter measured at $V_{CG} = 0$ V was approximately 2.8.

Introduction

Recently, organic thin-film transistors (OTFTs) have begun to attract attention as next generation electronic devices because of their ability to effect cost reduction, their flexibility, and their relatively small burden on the environment [1]. In particular, the characteristics and the performance of the pentacene field-effect transistors (FETs) have made such devices viable for stretchable e-skins applications requiring large area coverage and mechanical flexibility [2, 3]. However, despite their great potential, their performance so far has been limited by poor material quality originating from the many defects in organic materials and the large contact resistance. The problem of organic material's quality was mainly solved by the purification of a raw material [4, 5]. The reduction of contact resistance has been shown to be possible in experimental self-assembly monolayer treatments and in the reformation of the electrode process [6, 7].

This study reports on the electric characteristics of pentacene OTFTs with a double-gated structure. Pentacene is a well-known aromatic molecule and has shown field-effect mobility as large as 1.5 cm^2/Vs in earlier works by Lin et al. [8]. Many researchers such as Iba et al. have demonstrated that, with double-gated pentacene OTFTs, increased drain currents can be achieved as a consequence of top and bottom gates [9–12]. The double gate plays an important role in the reduction of contact resistance, and using such a gate has been successfully applied for the study of high-mobility Si MOS-FETs at low temperatures [13]. Two electrodes of the main and complementary gates are fabricated on opposite sides of a silicon oxide film and isolated from each other. The complementary gate electrode (closer to the pentacene) consists of a stripe that overlaps with the source contact. The resistance of Schottky barriers and the charge density in the channel of this device can be controlled separately by applying different voltages to the main and complementary gate electrodes. This study also describes the results of a Kelvin-probe force microscope (KFM) measurement and the complementary gate voltage dependency of an inverter.

Experimental procedures

Pentacene materials (Aldrich Chemical Co.) were purified using vacuum sublimation at 10^{-3} Torr or lower. The

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pentacene thin films were deposited in situ on Au(800 Å)/Ti(10 Å)/parylene(3000 Å)/Au(800 Å)/Ti(10 Å)/SiO_2(3000 Å)/Si structures by using a conventional thermal evaporator at a pressure below 10^{-6} Torr. The Si substrate—a heavily doped, thermally oxidized silicon wafer—was treated with hexamethyldisilazane (HMDS) as a self-organizing material, which compound was used to improve the quality of the organic/dielectric interface [14], and the system was maintained at 60 °C during the depositions. The deposition rate was about 1 Å/s. The thickness of the pentacene films was approximately 100 nm. The surface morphology of the pentacene films was examined with atomic force microscopy (AFM) and the dendritic grains in the films were observed. The parylene-c (poly-chloro-*p*-xylylene) film used as the gate dielectric material was deposited onto this structure using a sublimation and pyrolysis apparatus. The parylene-c dimmer was vaporized at approximately 100 °C and the samples were located on a cooled susceptor plate. Typical deposition rates were from 1 to 3 Å/s, and the thickness of the parylene-c films was approximately 3000 Å.

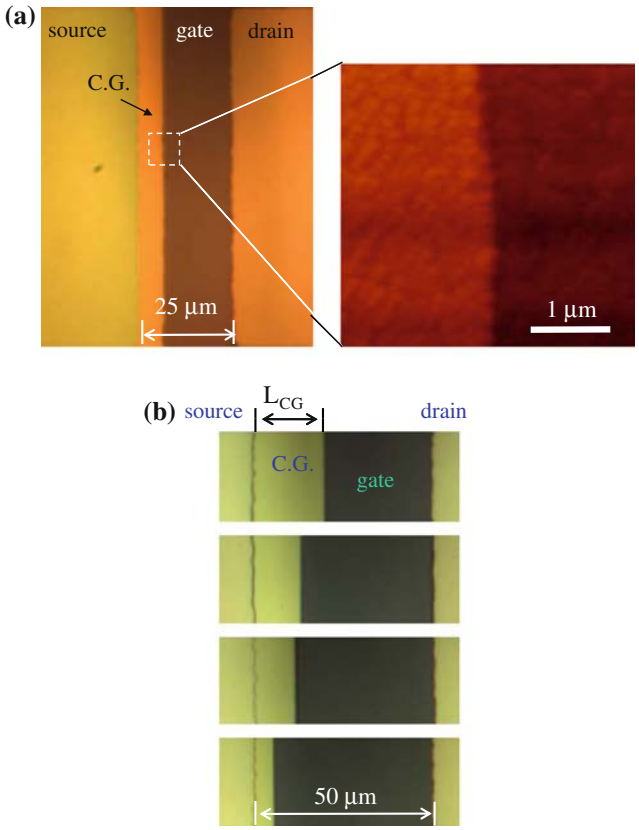

Fig. 1 **a** Photograph (*left side*) and AFM (*right side*) images for OTFTs. *C.G.* complementary gate. **b** Photograph images for OTFTs with different complementary gate lengths. The length and width of channel are 50 and 100 μm, respectively

Figure 1a shows the images of photograph and AFM for pentacene OTFTs with a double-gated structure. Drain current–drain voltage (I_D–V_D) and drain current–main gate voltage (I_D–V_G) characteristics of this sample were shown in Fig. 2. Figure 1b describes the photograph images for OTFTs with the different lengths of complementary gate electrode. Drain current–main gate voltage (I_D–V_G) curves of these samples were shown in Fig. 4. This result represented that the overlapped area of the complementary gate below 50% played an important part in the increase or decrease of the drain current. The structure of OTFTs that we used for this study is shown in the inset of Fig. 2a. The heavily doped, *n*-type silicon substrate acted as a main gate electrode, and thermal Si oxide and parylene layers acted as the gate dielectrics of OTFTs. The complementary gate

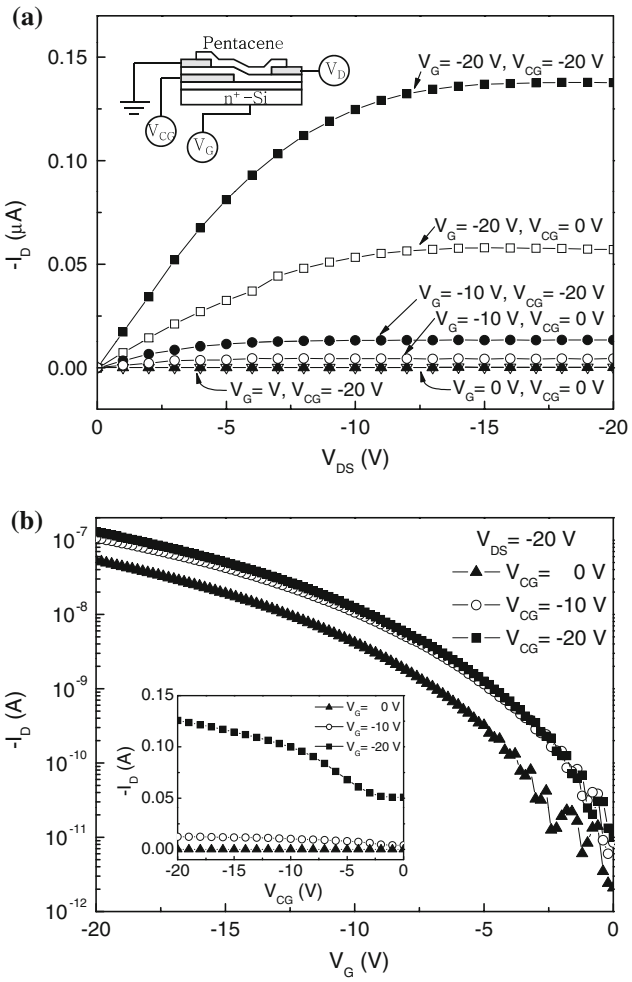

Fig. 2 **a** Drain current–drain voltage (I_D–V_D) curve of pentacene OTFTs (W/L = 100/25). The main and complementary gate voltages were changed between 0 and −20 V. **b** Drain current–main gate voltage (I_D–V_G) and drain voltage–complementary gate voltage (I_D–V_{CG}) characteristics of pentacene OTFTs. The drain voltage is −20 V, and the length (L) and width (W) of channel are 25 and 100 μm, respectively

electrode was fabricated between thermal silicon oxide and parylene layers. Analysis of the electronic property of OTFTs was conducted at room temperature using a Hewlett-Packard 4145B semiconductor parameter analyzer at various gate voltages. The profiles of surface potentials were measured with a KFM.

Results and discussion

Figure 2a shows the plot of drain current I_D versus drain voltage V_D at various main and complementary gate voltages (V_G and V_{CG}) for the pentacene OTFT with channel length (L) of 25 μm and width (W) of 100 μm. The voltages of main and complementary gates were changed between 0 and −20 V. When the gate electrode was biased negatively with respect to the grounded source electrode, OTFTs operated in an accumulation mode and the accumulated charges were holes. The trans-conductance characteristics of the drain current–main gate voltage (I_D–V_G) and drain voltage–complementary gate voltage (I_D–V_{CG}) at the drain voltage of −20 V for pentacene OTFTs are described in Fig. 2b. In the trans-conductance curves, the large negative voltage V_{CG} reduced the contact resistance between pentacene and the source Au electrode, and a regime of low carrier densities became easily accessible. This means that the portion of the pentacene surface on the complementary gate electrode is screened from the field of the main gate electrode [15]. Field-effect mobility, which was measured in the linear portion of the trans-conductance curves, was approximately 0.04 cm^2/Vs. On/off ratios of approximately 10^5 were achieved between I_D currents at $V_G = -20$ V and $V_G = 0$ V measured at a certain V_D in the saturation regime.

Figure 3 represents the surface morphology and potential profile of the pentacene films examined by KFM. The drain voltage V_D was −8 V, and the main and complementary gate voltages were changed between 0 and −20 V. In the case of $V_G = 0$ V and $V_{CG} = 0$ V, the one-dimensional potentials of pentacene OTFTs changed smoothly. On the other hand, those at $V_G = -20$ V and $V_{CG} = -20$ V decreased steeply around the source electrode. That is, as the amplitude of main and complementary gate voltages increased, the potential variation at the interface between source and pentacene were larger than those in the interior parts of channel. The surface morphology of OTFTs was discriminated from the regions of source, drain, and complementary gate electrodes. The screened length of the complementary gate electrode was approximately 12.5 μm, and the height of electrodes was approximately 50 nm. The root-mean-square surface roughness of the pentacene was approximately 55 Å. The inset of Fig. 3 shows the KFM results of the pentacene OTFTs having a conventional structure. This result was very similar to those reported by Palermo and other researchers [16, 17].

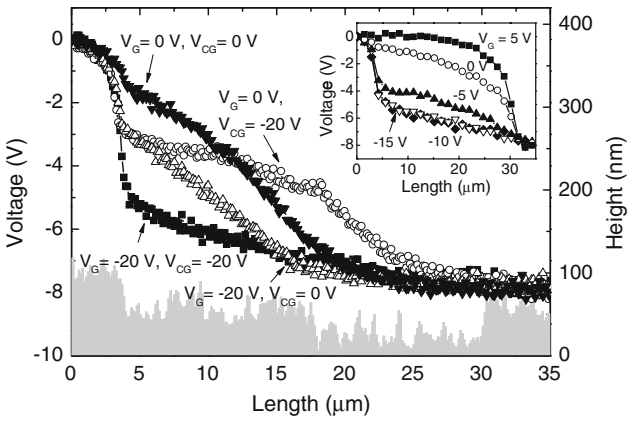

Fig. 3 One-dimensional potential profiles of pentacene OTFTs (W/L = 100/25). The main and complementary gate voltages were changed between 0 and −20 V. The *inset* is KFM results of the pentacene OTFTs having a conventional structure

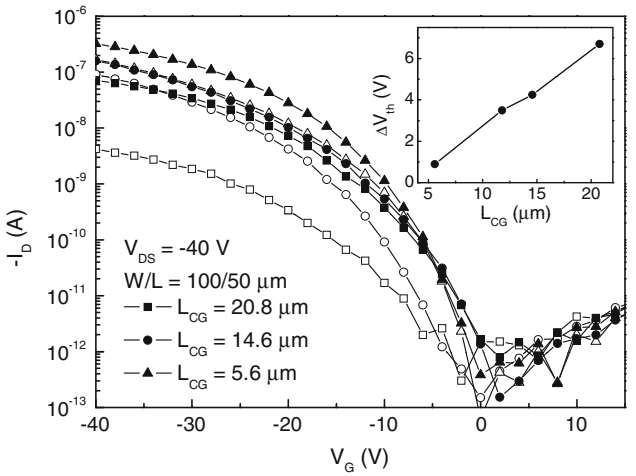

Fig. 4 Drain current–main gate voltage (I_D–V_G) characteristics for pentacene OTFTs (W/L = 100/50) with the different lengths of complementary gate electrode. The drain voltage is −20 V. The *open* and *filled symbols* are the cases of $V_{CG} = 0$ and −20 V, respectively

Figure 4 reveals the drain current–main gate voltage (I_D–V_G) characteristics for pentacene OTFTs with different lengths (L_{CG}) of complementary gate electrode. The channel length and width were 50 and 100 μm, respectively. The drain voltage was −40 V. The open and filled symbols are the cases of $V_{CG} = 0$ and −40 V, respectively. As the overlap region between main and complementary gate electrodes became larger, the effect of complementary gate voltages appeared to be more powerful. Especially, the drain current (I_D) of OTFTs with an overlap length of 20.8 μm at $V_G = -40$ V and $V_{CG} = 0$ decreased to a level of 10% of I_D at $V_G = -40$ V and $V_{CG} = -40$ V.

Figure 5 shows the input voltage–output voltage curves for a p-type metal-oxide semiconductor (pMOS) inverter of

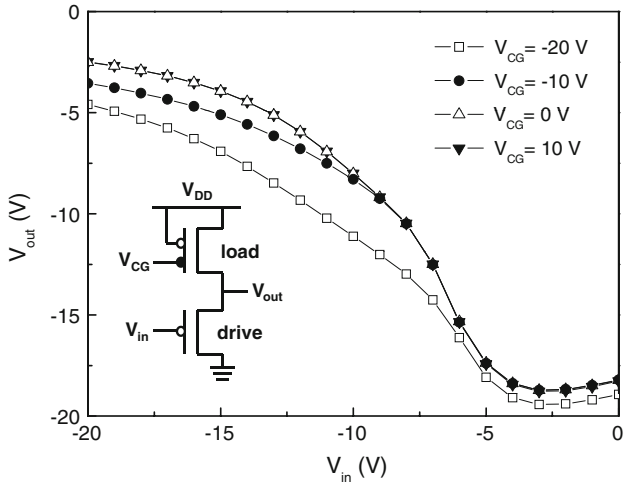

Fig. 5 Input–output curves of the inverter measured at various complementary gate voltages. The *inset* is the schematic diagram of a pMOS d-inverter constructed with conventional and double-gated OTFTs

depletion mode (d-inverter) operated at four complementary gate voltages ($V_{CG} = 10$, 0, -10, and -20 V). The inset of Fig. 5 is a schematic diagram of a pMOS d-inverter, which is constructed with conventional and double-gated OTFTs. The drive transistor was a conventional OTFT but the load transistor was a double-gated OTFT. The input voltage was scanned from 0 to -20 V, and V_{DD} was maintained at -20 V during the scan. When $V_{CG} = 0$ V, the low-level output voltage (when the input voltage was 0 V) was approximately -18 V and the high-level output voltage (when the input voltage was -20 V) was approximately 2.5 V. The observed gains of the inverter with a double-gated OTFT were from 2.8 to 2.1 in the range of $V_{CG} = 10$ and -20 V. The variation of gains might be caused by the difference of barrier height between source electrode and pentacene. The simple technique introduced here should be valuable in fabricating devices for integrated circuits, including flexible ones.

Conclusions

In summary, this study investigated the electric properties of pentacene OTFTs with main and complementary gate electrodes from I_D–V_D, I_D–V_G, and I_D–V_{CG} measurements. The structural and electronic properties of functional surfaces and interfaces for OTFTs were observed simultaneously by using a KFM apparatus. In these results, the different potential drops between source Au electrode and pentacene appeared as a function of the complementary gate voltages. We also designed and fabricated a pMOS d-inverter constructed with conventional and double-gated OTFTs, and the circuit properties of the inverter were measured. The gain of the d-inverter measured at $V_{CG} = 0$ V was approximately 2.8.

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